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Presented for filing is a new original patent application of:

Applicant: WILLIAM E. HOKE AND KATERINA Y. HUR

Title: DOUBLE RECESSED TRANSISTOR

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Enclosed are the following papers, including those required to receive a filing date under 37 CFR 1.53(b):

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Enclosures:
— Postcard.

Basic filing fee	$690
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APPLICATION

FOR

UNITED STATES LETTERS PATENT

TITLE: DOUBLE RECESSED TRANSISTOR

APPLICANT: WILLIAM E. HOKE AND KATERINA Y. HUR

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DOUBLE RECESSED TRANSISTOR

Background of the Invention

This invention relates generally to high electron mobility transistors (HEMTs) and more particularly to transistors of such type which are fabricated with a double recess.

As is known in the art, there are several types of active devices used at microwave and millimeter frequencies to provide amplification of radio frequency signals. In general, one of the more common semiconductor devices used at these frequencies is the high electron mobility transistor (HEMT). Typically, HEMTs are formed from Group III-V materials such as gallium arsenide (GaAs) or indium phosphide (InP). In a HEMT there is a doped donor/undoped spacer layer of one material and an undoped channel layer of a different material. A heterojunction is formed between the doped donor/undoped spacer layer and the undoped channel layer. Due to the conduction band discontinuity at the heterojunction, electrons are injected from the doped donor/undoped spacer layer into the undoped channel layer. Thus, electrons from the large bandgap donor layer are transferred into the narrow bandgap channel layer where they are confined to move only in a plane parallel to the heterojunction. Consequently, there is spatial separation between the donor atoms in the donor layer and the electrons in the channel layer resulting in low impurity scattering and good electron mobility.

One device which has been found to provide good device characteristics such as breakdown voltage, output currents, and pinch-off voltage is a double recessed HEMT. Such a device is fabricated with two aligned recesses in

which the gate is formed. The recesses are typically formed by wet etching the device. For example, etching the recesses can include selective and non-selective etching. For non-selective etching, the process is periodically interrupted and the device is tested for certain characteristics, e.g., current. If the characteristics meet the desired criteria, then etching for the recess is terminated. Otherwise, the etching continues. This non-selective process continues until the recess meets the established criteria. This process takes time and money to repeatedly stop the etching and test the device. Also, the etching is not uniform across the wafer, resulting in inconsistent device characteristics across the wafer and low yield of acceptable devices on the wafer.

Summary of the Invention

In accordance with the present invention, a transistor structure is provided. This structure has a source electrode and a drain electrode. A doped cap layer of $Ga_xIn_{1-x}As$ is disposed below and in ohmic contact with the source electrode and the drain electrode and provides a cap layer opening. An undoped resistive layer of $Ga_xIn_{1-x}As$ is disposed below the cap layer and provides a resistive layer opening in registration with the cap layer opening and having a first width. A Schottky layer of $Al_yIn_{1-y}As$ is disposed below the resistive layer. An undoped channel layer is disposed below the Schottky layer. A semi-insulating substrate is disposed below the channel layer. A top surface of the Schottky layer beneath the resistive layer opening provides a recess having a second width smaller than the first width. A gate electrode is in contact with a bottom

surface of the recess provided by the Schottky layer.

With such structure, uniform device characteristics such as breakdown voltage, output currents, and pinch-off voltage are achievable, as is a high yield of acceptable devices.

In accordance with another feature of the invention, a semiconductor structure is provided having a Schottky layer adapted to be etched at a first etch rate by an etchant. The semiconductor structure also has a contact layer disposed above the Schottky layer and adapted to be etched by the etchant at a second etch rate that is substantially faster than the first etch rate. The contact layer provides an opening exposing a region of a top surface of the Schottky layer, the region having a first width. The region of the top surface of the Schottky layer provides a recess of a second width smaller than the first width.

In a preferred embodiment of the invention, the Schottky layer contains aluminum, with an etch rate of about 0.1Å/second relative to a succinic acid etchant, while the contact layer is substantially free of aluminum, having an etch rate of about 5Å/second relative to succinic acid etchant. Such composition allows the transistor's contact layer to be selectively etched with succinic acid to form the opening while leaving the Schottky layer substantially intact. Thus, uniform device characteristics such as breakdown voltage, output currents, and pinch-off voltage can be achieved and a high yield of acceptable devices produced.

In accordance with another feature of the invention, a transistor structure is provided having a Schottky layer adapted to be etched at a first etch rate by an

etchant and a contact layer disposed above the Schottky layer and adapted to be etched by the etchant at a second etch rate that is substantially faster than the Schottky layer's first etch rate. In this structure, a region above a portion of a top surface of the Schottky layer is substantially free of the contact layer. The portion of the top surface of the Schottky layer has a first width and provides a recess having a second width smaller than the first width and adapted to receive a gate electrode.

In a preferred embodiment of the invention, the Schottky layer comprises at least about 35 percent Aluminum and the contact layer comprises less than about ten percent Aluminum.

In accordance with another feature of the invention, a double recessed, strain compensated transistor structure is provided. The semiconductor structure has a substrate, a strain compensating layer disposed above the substrate, and a Schottky layer disposed above the strain compensating layer. The substrate and the layers have mismatched lattice constants.

In a preferred embodiment of the invention, the Schottky layer comprises about 60 percent aluminum and about 40 percent indium, and the strain compensating layer comprises about 35 percent gallium and 65 percent indium.

In accordance with another feature of the invention, a method of forming a semiconductor is provided. The method includes forming a Schottky layer adapted to be etched by a first etchant at a first etch rate and forming a contact layer above the Schottky layer adapted to be etched by the first etchant at a second etch rate that is substantially

faster than the first etch rate. The first etchant is applied to etch the contact layer to expose a portion of the Schottky layer. A second etchant is applied to etch the portion of the Schottky layer exposed by the first etchant.

In a preferred embodiment of the invention, the Schottky layer contains Aluminum while the contact layer is substantially free of Aluminum. Further, the first etchant includes a carboxylic-acid based wet etchant.

Embodiments of the invention may provide one or more of the following advantages. The invention saves time and money in manufacturing HEMTs. It also decreases the need to etch a device and periodically test the device for certain characteristics. Uniformity of device characteristics on a wafer can be improved.

Other advantages will be apparent from the following description and from the claims.

Brief Description of the Drawings

FIG. 1 is a cross sectional diagrammatical sketch of a double recessed HEMT according to the invention;

FIGS. 2-4 are cross sectional diagrammatical sketches of the double recessed HEMT of FIG. 1 in various stages of manufacture; and

FIG. 5 is a cross sectional diagrammatical sketch of a double recessed, strain compensated HEMT according to the invention.

Description of Preferred Embodiments

Referring now to FIG. 1, a high electron mobility transistor (HEMT) 10 is shown. Here, transistor 10 has a source electrode 12 and a drain electrode 14. The electrodes 12 and 14 are in ohmic contact with a cap layer 16. The cap

layer 16 here is $Ga_{0.47}In_{0.53}As$, about 70D thick, and has a doping concentration of about $5x10^{18}$ cm^{-3}. Disposed below the cap layer 16 is a recess or resistive layer 18. The resistive layer 18 here is $Ga_{0.47}In_{0.53}As$, about 300D thick, and undoped. The cap and resistive layers 16 and 18 form a contact layer 50. Disposed below the resistive layer 18 is a Schottky layer 20, here undoped $Al_{0.60}In_{0.40}As$ about 200D thick. The cap and resistive layers 16, 18 provide an opening 38 from a surface 56 to a top surface 42 of the Schottky layer 20. The top surface 42 of the Schottky layer 20 provides a recess 44 with a bottom surface 48. In Schottky contact with the Schottky layer 20 at the bottom surface 48 is a gate electrode 22. A doped pulse layer 24 is disposed below the Schottky layer 20. Here the pulse layer 24 is silicon and has a doping concentration of about $2x10^{12}$ cm^{-2}. Disposed below the pulse layer 24 is a spacer layer 26. The spacer layer 26 here is $Al_{0.48}In_{0.52}As$, about 30D thick, and undoped. Disposed below the spacer layer 26 is a channel layer 28. The channel layer 28 here is $Ga_{0.47}In_{0.53}As$, about 200D thick, and undoped. A second spacer layer 30 is disposed below the channel layer 28. Here the spacer layer 30 is $Al_{0.48}In_{0.52}As$, about 50D thick, and undoped. Disposed below the spacer layer 30 is a second pulse layer 32. Here the pulse layer 32 is silicon and has a doping concentration of $1x10^{12}$ cm^{-2}, providing a silicon pulse ratio of 2:1 between the first pulse layer 24 and the second pulse layer 32 to help linearize the performance of the transistor 10. Disposed below the pulse layer 32 is a buffer layer 34. The buffer layer 34 here is $Al_{0.48}In_{0.52}As$, about 2000D thick, and undoped. Disposed below the buffer layer 34 is a semi-insulating InP

substrate 36.

The Schottky layer 20 can be undoped, as shown, or doped. An undoped Schottky layer provides a higher breakdown voltage than with a doped Schottky layer 20. A doped Schottky layer 20 reduces resistance which lowers the breakdown voltage and increases conduction compared to an undoped Schottky layer 20.

As shown, transistor 10 has a double recess structure including a first recess 39, formed by the opening 38 and the top surface 42 of the Schottky layer 20, and the second recess 44. The first recess 39 is provided by the cap layer 16 and the resistive layer 18. Side walls 40 of the first recess 39 are provided by the cap and resistive layers 16, 18 from the surface 56 to the top surface 42 of the Schottky layer 20. The first recess 39 exposes a first width W1 of the Schottky layer 20 at a top level 43 of the Schottky layer 20. The second recess 44 has a second width W2 at the bottom surface 48, the width W2 being smaller than the width W1. The second recess 44 is provided by the top surface 42 of the Schottky layer 20 and has side walls 46 extending from the top 43 of the Schottky layer 20 to the bottom surface 48.

The cap and resistive layers 16, 18 have different material composition than the Schottky layer 20. The Schottky layer 20 includes Group III-V material, here aluminum and indium. Sixty percent of the Group III material in the Schottky layer 20 is aluminum and forty percent is indium. To provide desirable device characteristics, there is preferably at least 35 percent aluminum in the Schottky layer 20, and less than about ten percent aluminum in the cap and resistive layers 16, 18. The cap and resistive layers

16, 18 are preferably substantially free of Aluminum, though they can contain up to about ten percent Aluminum and still provide desirable device characteristics.

The cap and resistive layers 16, 18 have a different etch rate than the Schottky layer 20 to provide etch selectivity. The Schottky layer 20 is adapted to be etched at a first etch rate by an etchant. The $Al_{0.60}In_{0.40}As$ Schottky layer 20 shown has an etch rate of about 0.1Å/second when exposed to an etchant of succinic acid, which is a carboxylic-acid based wet etchant. The cap and resistive layers 16, 18 are adapted to be etched by the etchant at a second etch rate that is substantially faster than the first etch rate. The $Ga_{0.47}In_{0.53}As$ layers 16, 18 have etch rates of about 5Å/second when etched by succinic acid.

A method of forming a semiconductor device such as transistor 10 is now described, referring to FIGS. 1-4. FIG. 2 shows the forming of layers 16, 18, and 20. FIGS. 3 and 4 show the etching of layers 16, 18, and 20. FIG. 1 shows the finished transistor 10.

The method of forming transistor 10 in FIG. 1 includes forming the Schottky layer 20 and the cap and resistive layers 16, 18 above the Schottky layer 20. An etchant is applied to the cap and resistive layers 16, 18 to etch them and expose the top surface 42 of the Schottky layer 20. Another etchant is applied to etch the exposed top surface 42 of the Schottky layer 20 to produce the recess 44.

Referring to FIG. 2, forming the semiconductor layers 16, 18, and 20 is now described. As shown in FIG. 2, the substrate 36 is provided and the buffer layer grown on the substrate 36 by suitable techniques such as molecular beam

epitaxy (MBE) and metal-organic chemical vapor deposition (MOCVD). Over the buffer layer 34 the pulse layer 32 is grown by MBE and doped by silicon. Over the pulse layer 32 the spacer layer 30, the channel layer 28, and the spacer layer 26 grown by MBE. Over the spacer layer 26 the pulse layer 24 is grown by MBE and doped by silicon. Over the pulse layer 24 the Schottky layer 20 is grown by MBE. Referring now to FIG. 3, the contact layer 50, including the cap layer 16 and the resistive layer 18, is formed by MBE on the Schottky layer 20 to complete the formation of an intermediate structure 54. A wet etch process for mesa isolation is performed by applying 1:8:160 H_2SO_4:H_2O_2:H_2O for about 20 seconds to define the mesa. Then, 6:1 succinic acid:H_2O_2 is applied for about 90 seconds to selectively etch back the InGaAs channel layer 28. This forms a channel notch (not shown) to help prevent shorting of the channel layer 28 to the gate electrode 22 via a conductor (not shown) running up the side of the mesa.

Referring to FIGS. 3 and 4, etching the intermediate structure 54 is now described. As shown in FIG. 3, a first etchant, here a carboxylic-acid based wet etchant, specifically 6:1 succinic acid:H_2O_2 is applied to the top surface 56 of the cap layer 16. Electron beam lithography is used with the succinic acid and the succinic acid is applied for enough time, e.g., about 60 seconds, to etch the contact layer 50 at the second etch rate to form the opening 38. This exposes the top surface 42 of the Schottky layer 20, selectively forms the first recess 39, and completes the formation of an intermediate structure 58. Because the first etch rate of the Schottky layer 20 is substantially slower

than the second etch rate of the contact layer 50 in response to the succinic acid, the succinic acid essentially does not etch the Schottky layer 20. The first etch is a selective etch.

Now referring to FIG. 4, intermediate structure 58 is etched. A second etchant, e.g., 1:1:100 H_3PO_4:H_2O_2:H_2O is applied to a portion of the top surface 42 of the Schottky layer 20 exposed by the succinic acid for enough time to etch the Schottky layer 20, e.g., 10 seconds. This etching forms the second recess 44, and completes the formation of intermediate structure 60.

Referring to FIG. 1, electrodes 12, 14, and 22 are added to the intermediate structure 60 to complete the transistor 10. The source and drain electrodes 12 and 14 are in ohmic contact with the top surface 56 of the cap layer 16. These ohmic contacts for the source and drain electrodes 12 and 14 are fabricated using a 900D AuGe-2000D Au metallurgy at 375EC. The gate electrode 22 is in Schottky contact with the bottom surface 48 of the Schottky layer 20. The gate recess is formed by depositing a resist layer, not shown. The resist is developed and removed according to known methods (e.g., by exposing a photoresist, removing the photoresist), and then the recess is formed by etching the semiconductor. Schottky metal of 500Å Ti-500Å Pt-4000Å Au is deposited over the resist layer on the recess 44. The resist layer is lifted off to remove unwanted metal, leaving the gate electrode 22.

The transistor 10 shown in FIG. 1 has been fabricated and tested. The transistor 10 had a typical carrier sheet density of about $3x10^{12}$ cm^{-2}, Hall mobility of 8300 cm^2/V-sec

at room temperature, maximum output current in the range 590-640 mA/mm, and breakdown voltage in the range 12.3-14.4 V.

In another embodiment of the invention, referring now to FIG. 5, a double recessed, strain compensated HEMT is provided. The HEMT 100 includes a semi-insulating, single crystal InP substrate 102. The substrate 102 has an inherent lattice constant. Disposed above the substrate 102 is an undoped buffer layer 104 lattice matched to the substrate 102. The buffer layer 104 here is $Al_{0.48}In_{0.52}As$, having a thickness of 1,500-5,000Å, typically about 2000Å. Disposed above the buffer layer 104 is a first pulse layer 106, also called a ä-doped or pulse doped layer. The pulse layer 106 is silicon and has a doping concentration of $0.5x10^{12}$-$2x10^{12}$ cm^{-2}, typically $1x10^{12}$ cm^{-2}. Disposed above the first pulse layer 106 is a first spacer layer 108. The first spacer layer 108 is $Al_{0.48}In_{0.52}As$, having a thickness of 30-50Å, preferably about 50Å thick, and undoped.

Disposed over the first spacer layer 108 is the channel layer 110 having an inherent lattice constant. The lattice constant of the channel layer 110 is different than the lattice constant of the substrate 102. The channel layer 110 serves as a strain compensation layer, comprised of a material which will develop an inherent or intrinsic compressive strain when grown over the first spacer layer 108 due to lattice constant mismatch between the channel layer 110 and the substrate 102. Here, the material used for the channel layer 110 is $Ga_{1-x}In_xAs$, with an indium concentration, x, of 0.53-0.70, preferably 0.60-0.65. The channel layer 110 has a thickness of 50-400Å, preferably about 200Å thick, and is undoped. The thickness of the channel layer 110 is a

function of the indium concentration in the channel layer 110, since the indium concentration in the channel layer 110 affects the lattice constant (and strain) of the channel layer 110. As the indium concentration changes, the lattice constant of the channel layer also changes, thereby affecting the degree of lattice mismatch between the channel layer 110 and other layers in the HEMT 100. The greater the lattice mismatch, the thinner the channel layer 110 will be to avoid dislocations in the channel layer 110. In general, the composition and thickness of the channel layer 110 is selected to provide a layer having an intrinsic compressive stress which substantially compensates for intrinsic tensile stress of a Schottky layer 116 disposed over the channel layer 110, as described below. The thickness and indium concentration of the channel layer 110 are selected to maximize that compensating effect while avoiding dislocations in the channel layer 110, and consequently do not exceed the elastic strain limits of the channel layer 110.

First, disposed above the channel layer 110 is a second spacer layer 112. The second spacer layer 112 here is $Al_{0.48}In_{0.52}As$, about 30-50Å thick, and undoped. Disposed above the second spacer layer 112 is a second pulse layer 114, also called a ä-doped or pulse doped layer. The second pulse layer 114 is silicon and has a doping concentration of about $2x10^{12}$-$4x10^{12}$ cm^{-2}, preferably $3x10^{12}$ cm^{-2}, typically providing a ratio of doping concentrations between the first pulse layer 106 and the second pulse layer 114 of approximately 2.5 to 1.5 to help linearize performance of the transistor 100.

Disposed above the second pulse layer 114 is the Schottky layer 116 having an inherent lattice constant. The

lattice constant of the Schottky layer 116 is different than the lattice constants of the channel layer 110 and of the substrate 102. That is, these three layers are not lattice matched. Typically, the lattice constant of the Schottky layer 116 is smaller than the lattice constant of the substrate 102, and the lattice constant of the channel layer 110 is larger than the lattice constant of the substrate 102. Here, the Schottky layer 116 is $Al_{1-x}In_xAs$ with an aluminum concentration, 1-x, of 0.55-0.65, preferably 0.60. The Schottky layer 116 has a thickness of 50-400Å, preferably about 200Å thick, and is undoped. The thickness of the Schottky layer 116 will depend on the indium concentration in the Schottky layer 116. As the indium concentration changes, the lattice constant (and strain) of the Schottky layer also changes. Similar to the channel layer 110, the thickness and indium concentration of the Schottky layer 116 are balanced and maximized while avoiding dislocations due to lattice mismatch. Here, the Schottky layer 116 is undoped. An undoped Schottky layer provides a higher breakdown voltage than with a doped Schottky layer. A doped Schottky layer reduces resistance which lowers the breakdown voltage and increases conduction compared to an undoped Schottky layer. The growth of the Schottky layer provides a layer having tensile strain due to the lattice mismatch between the Schottky layer 116 and the underlying layers.

By disposing the channel or strain compensation layer 110 between the buffer layer 104 and the Schottky layer 116, the Schottky layer 116 may be grown to a larger thickness than if the Schottky layer 116 were grown directly on the buffer layer 104. Alternatively, the aluminum concentration

in the Schottky layer 116 may be increased or any combination of the aforementioned arrangements may be provided to form the Schottky layer. Insertion of the channel layer 110 permits a thicker Schottky layer 116 or alternatively a higher concentration of aluminum in said Schottky layer 116 before the Schottky layer 116 reaches a sufficiently high enough tensile strain to cause dislocations in the crystal lattice of said Schottky layer 116. With the above arrangement, the channel layer 110 is grown to a thickness approaching, but not exceeding, a critical thickness of the channel layer 110. The Schottky layer 116 is grown over the channel layer 110. The initial growth of the Schottky layer 116 would provide a layer having tensile strain which would be compensated for by the compressive strains in the underlying channel layer 110. After the Schottky layer 116 is grown to a first thickness of zero net strain (i.e. compensated for by the compressive strain of the channel layer), the Schottky layer 116 is grown to an additional thickness until the Schottky layer additional thickness reaches a so-called critical thickness of the layer. By either incorporating additional aluminum into the Schottky layer 116 or by increasing the thickness of the Schottky layer 116, a higher bandgap for breakdown is achieved. Similarly, the tensile strain in the Schottky layer 116 stabilizes the high indium concentration in the channel layer 110. High indium concentration permits higher electron mobility and higher electron saturation velocity, thereby improving the overall performance of the HEMT 100 and permitting the HEMT 100 to handle larger amount of currents and thus power at higher frequencies. Further, an increase

in aluminum concentration in the Schottky layer 116 and/or a higher indium concentration in the channel layer 110 increases the conduction band discontinuity between the Schottky 116 and channel 110 layers. This increases the current sheet density which also improves power performance.

Disposed over the Schottky layer 116 is a resistive layer 118. The resistive layer 118 here is $Al_{0.48}In_{0.52}As$, about 50-400Å thick, typically 200Å thick, and undoped. Disposed over the resistive layer 118 is a contact layer 120. The contact layer 120 here is $Ga_{0.47}In_{0.53}As$, about 100-500Å thick, typically 70Å thick, and has a doping concentration of about $3x10^{18}$-$5x10^{19}$ cm^{-3}.

The contact and resistive layer 120, 118 provide an opening 124 from a surface 126 to a top surface 128 in the resistive layer 118. The top surface 128 provides a recess 130 with a bottom surface 132. In Schottky contact with the Schottky layer 116 at the bottom surface 132 is a gate electrode 134. The transistor 100 has a source electrode 136 and a drain electrode 138. The electrodes 136 and 138 are in ohmic contact with a cap layer 120.

As shown in FIG. 5, transistor 100 has a double recess structure including a first recess 140, formed by the opening 124 and the top surface 128, and the second recess 130. The first recess 140 is provided by the contact layer 120 and the top of the resistive layer 118. Side walls 142 of the first recess 140 are provided by the contact layer 120. The first recess 140 exposes a first width W10 of the resistive layer 118. The second recess 130 has a second width W20 at the bottom surface 132, the width W20 being smaller than the width W10. The second recess 130 is

provided by the top surface 128 of the resistive layer 118 and has side walls 144 extending from the top surface 128 to the bottom surface 132 in the Schottky layer 116.

The recesses are fabricated by selective and non-selective wet etching. Typically, the first recess is fabricated by selective etching, with the resistive layer 118 acting as an etching stop. The second recess is fabricated by non-selective etching. The wet etching for mesa isolation with a channel notch consists of a 20 sec. etch in 1:8:160 $H_2SO_4:H_2O_2:H_20$ and a 90 sec. etch in a 6:1 succinic acid:H_2O_2 etchant. Ohmic contacts for source and drain pads are fabricated using a 900Å AuGe - 2000Å Au metallurgy and 375 EC alloy furnace. A succinic acid etchant and a 1:1:100 $H_3PO_4:H_2O_2:H_2O$ etchant are used for the first recess and a gate etch, respectively. After the gate recess etch, Schottky metal consisting of 500Å Ti - 500Å Pt - 4000Å Au is deposited and lifted off.

The strain compensated, double recessed HEMT 100 shown in FIG. 5 has been fabricated and tested. The tensile strain in the Schottky layer 116 is compensated by the compressive strain in the channel layer 110. This strain compensation allows the Schottky layer 116 to be grown thicker or to be grown with higher aluminum concentration than if the Schottky layer were lattice matched with the underlying layers. The use of higher indium concentration in the channel layer 110, because of strain compensation in the Schottky layer 116, increases the unity current gain cutoff frequency. Because of the larger conduction band discontinuity between the Schottky 116 and channel 110 layers (than had the layers been lattice matched), high output

currents are obtained. Low breakdown voltages from the high indium concentration in the channel layer 110 are alleviated by the use of a double recessed gate process. The transistor 100 exhibits high output current (690 - 850 mA/mm) and high breakdown voltages (9 -11 V) simultaneously. Due to the high indium concentration in the channel, the peak unity current gain cutoff frequency approaches 200GHz and 160 GHz for devices with first recess widths of 0.8 ìm and 1.2 ìm, respectively. Typical carrier sheet density is $4x10^{12}$ cm^{-2} and Hall mobility is 9600 cm^2/V-sec at room temperature.

Other embodiments are within the spirit and scope of the appended claims. For example, the contact layer 50 can be a single layer, doped or undoped.

What is claimed is:

1. A semiconductor structure comprising:

a Schottky layer adapted to be etched at a first etch rate by an etchant; and

a contact layer disposed above the Schottky layer and adapted to be etched by the etchant at a second etch rate that is substantially faster than the first etch rate;

wherein the contact layer provides an opening through the contact layer exposing a region of a top surface of the Schottky layer, the region having a first width; and

wherein the region of the top surface of the Schottky layer provides a recess of a second width smaller than the first width.

2. The semiconductor recited in claim 1 wherein the Schottky layer contains Aluminum.

3. The semiconductor recited in claim 2 wherein the Schottky layer comprises at least about 35 percent Aluminum.

4. The semiconductor recited in claim 3 wherein the Schottky layer is $Al_{0.6}In_{0.4}As$.

5. The semiconductor recited in claim 1 wherein the contact layer comprises less than about ten percent Aluminum.

6. The semiconductor recited in claim 1 wherein the contact layer is substantially free of Aluminum.

7. A transistor structure comprising:

a Schottky layer adapted to be etched at a first etch

rate by an etchant; and

a contact layer disposed above the Schottky layer and adapted to be etched by the etchant at a second etch rate that is substantially faster than the first etch rate;

wherein a region above a portion of a top surface of the Schottky layer is substantially free of the contact layer, the portion having a first width;

wherein the portion of the top surface of the Schottky layer provides a recess of a second width smaller than the first width; and

wherein the recess of the second width is adapted to receive a gate electrode.

8. The transistor recited in claim 7 wherein the Schottky layer comprises at least about 35 percent Aluminum and the contact layer comprises less than about ten percent Aluminum.

9. A method of forming a semiconductor comprising:

forming a Schottky layer adapted to be etched by a first etchant at a first etch rate;

forming a contact layer above the Schottky layer adapted to be etched by the first etchant at a second etch rate;

applying the first etchant to etch the contact layer to expose a portion of the Schottky layer; and

applying a second etchant to etch the portion of the Schottky layer exposed by the first etchant;

wherein second etch rate is substantially faster than the first etch rate when using the first etchant.

10. The method recited in claim 9 wherein the Schottky layer contains Aluminum.

11. The method recited in claim 10 wherein the Schottky layer comprises about 35 percent Aluminum.

12. The method recited in claim 11 wherein the contact layer is substantially free of Aluminum.

13. The method recited in claim 11 wherein the first etchant includes a carboxylic-acid based wet etchant.

14. The method recited in claim 13 wherein the first etchant is succinic acid.

15. The method recited in claim 11 wherein the second etchant is applied for a predetermined time.

16. A transistor structure comprising:

a source electrode;

a drain electrode;

a doped cap layer of $Ga_xIn_{1-x}As$ disposed below and in ohmic contact with the source electrode and the drain electrode and providing a cap layer opening;

an undoped resistive layer of $Ga_xIn_{1-x}As$ disposed below the cap layer and providing a resistive layer opening in registration with the cap layer opening and having a first width;

a Schottky layer of $Al_yIn_{1-y}As$ disposed below the

resistive layer;

an undoped channel layer disposed below the Schottky layer; and

a semi-insulating substrate disposed below the channel layer;

wherein a top surface of the Schottky layer beneath the resistive layer opening provides a recess having a second width smaller than the first width; and

wherein a gate electrode is in contact with a bottom surface of the recess provided by the Schottky layer.

17. The transistor recited in claim 16 wherein the Schottky layer is doped.

18. A transistor, comprising:

a single crystal substrate having a lattice constant;

a channel layer disposed over the substrate, the channel layer having a lattice constant different from the lattice constant of the substrate;

a Schottky layer disposed over the channel layer, the Schottky layer having a lattice constant different from the lattice constant of the substrate;

a resistive layer disposed over the Schottky layer; and

a contact layer disposed over the resistive layer, the contact layer having a first recess therein, such first recess having a bottom surface terminating in a top surface of the resistive layer;

a second recess having sidewalls in the

resistive layer and the Schottky layer, such second recess having a bottom surface terminating in the Schottky layer.

19. The transistor recited in claim 18 wherein the lattice constant of the Schottky layer and a thickness of the Schottky layer are selected to compensate for differences in strain between: (a) the channel layer and the substrate; and, (b) the Schottky layer and the substrate.

20. The transistor recited in claim 19 wherein the lattice constant of the Schottky layer is smaller than the lattice constant of the substrate and the lattice constant of the channel layer is larger than the lattice constant of the substrate.

21. The transistor recited in claim 20 wherein the lattice constant of the substrate is intermediate the lattice constant of the channel layer and the lattice constant of the Schottky layer, the difference in lattice constants resulting in a compressive strain on the channel layer and a tensile strain on the Schottky layer.

22. The transistor recited in claim 18 wherein the Schottky layer has an indium concentration and the indium concentration in the Schottky layer is lower than an indium concentration in the channel layer.

23. The transistor recited in claim 22 wherein the substrate comprises indium phosphide.

24. The transistor recited in claim 22 wherein the Schottky layer comprises approximately $Al_{0.60}In_{0.40}As$.

25. The transistor recited in claim 22 wherein the channel layer comprises approximately $Ga_{0.35}In_{0.65}As$.

26. The transistor recited in claim 23 wherein the Schottky layer comprises approximately $Al_{0.60}In_{0.40}As$ and the channel layer comprises approximately $Ga_{0.35}In_{0.65}As$.

27. A transistor, comprising;

a substrate having a lattice constant;

a channel layer disposed over the substrate, the channel layer having a lattice constant;

a Schottky layer disposed over the channel layer, the Schottky layer having a lattice constant;

a resistive layer disposed over the Schottky layer; and

a contact layer disposed over the resistive layer, the contact layer having a first recess therein, such first recess having a bottom surface terminating in a top surface of the resistive layer; and

a second recess having sidewalls in the resistive layer and the Schottky layer, such second recess having a bottom surface terminating in the Schottky layer;

wherein at least one of the channel and Schottky layers has an indium concentration such that at least one of the lattice constants of the channel layer and lattice constant of the Schottky layer is different from the lattice constant of the substrate and a difference between conduction

band levels of the channel and Schottky layers is larger than if the channel and Schottky layers had the same lattice constant as the substrate.

28. The transistor recited in claim 27 wherein the larger conduction band discontinuity occurs between the Schottky and channel layers.

29. The transistor recited in claim 27 wherein the Schottky layer comprises approximately $Al_{0.60}In_{0.40}As$ and the channel layer comprises approximately $Ga_{0.35}In_{0.65}As$.

30. The transistor recited in claim 25 wherein the channel layer has an indium concentration such that the channel layer can support larger currents than if the channel layer and the substrate had the same lattice constant.

31. A transistor, comprising:

a semi-insulating indium phosphide substrate;

a channel layer of $Ga_xIn_{1-x}As$ disposed over the substrate layer;

a Schottky layer of $Al_yIn_{1-y}As$ disposed over the channel layer;

a resistive layer disposed over the Schottky layer;

a contact layer disposed over the resistive layer, the contact layer having a first recess, and the resistive layer and the Schottky layer having a second recess;

a source electrode in ohmic contact with the contact layer;

a drain electrode in ohmic contact with the contact layer; and

a gate electrode in Schottky contact with the Schottky layer.

32. The transistor recited in claim 31 further comprising a first doped layer, and a second doped layer.

33. The transistor recited in claim 32 further comprising a ratio of silicon doping concentration approximately 2.5 to 1.5 between the first doped layer and the second doped layer.

34. The transistor recited in claim 32 wherein the resistive layer further comprises approximately $Al_{0.48}In_{0.52}As$ and the contact layer further comprises approximately $Ga_{0.47}In_{0.53}As$.

DOUBLE RECESSED TRANSISTOR

Abstract of the Disclosure

A transistor structure is provided. This structure has a source electrode and a drain electrode. A doped cap layer of $Ga_xIn_{1-x}As$ is disposed below the source electrode and the drain electrode and provides a cap layer opening. An undoped resistive layer of $Ga_xIn_{1-x}As$ is disposed below the cap layer and defines a resistive layer opening in registration with the cap layer opening and having a first width. A Schottky layer of $Al_yIn_{1-y}As$ is disposed below the resistive layer. An undoped channel layer is disposed below the Schottky layer. A semi-insulating substrate is disposed below the channel layer. A top surface of the Schottky layer beneath the resistive layer opening provides a recess having a second width smaller than the first width. A gate electrode is in contact with a bottom surface of the recess provided by the Schottky layer.

393823.B11

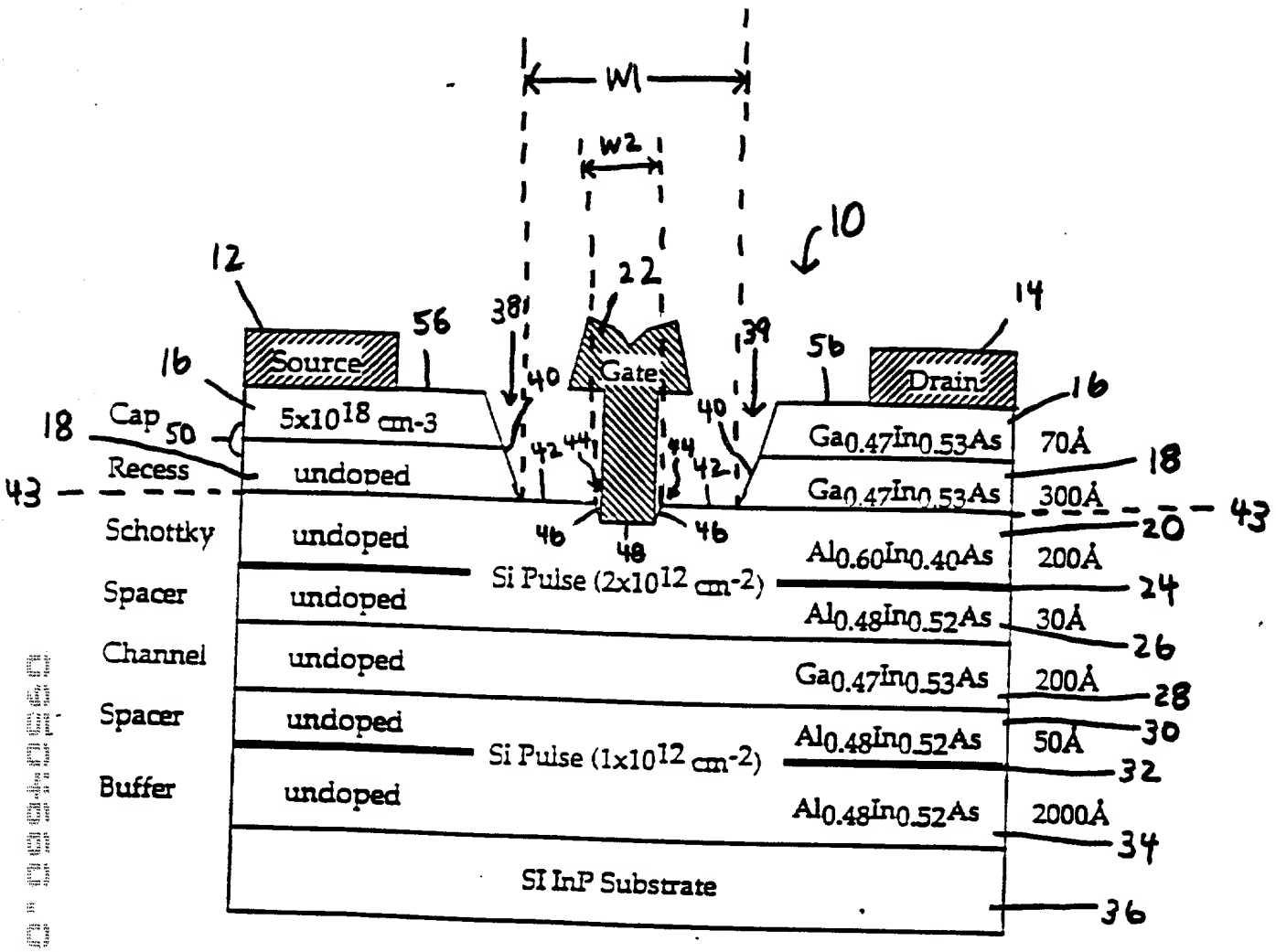
W1
W2
10
12
22
14
56
38
39
56
16
Source
Gate
Drain
16
18
Cap
50
5x10^18 cm-3
Ga0.47In0.53As
70Å
18
Recess
undoped
Ga0.47In0.53As
300Å
43
43
20
Schottky
undoped
Al0.60In0.40As
200Å
Si Pulse (2x10^12 cm-2)
24
Spacer
undoped
Al0.48In0.52As
30Å
26
Channel
undoped
Ga0.47In0.53As
200Å
28
Spacer
undoped
Al0.48In0.52As
50Å
30
Si Pulse (1x10^12 cm-2)
32
Buffer
undoped
Al0.48In0.52As
2000Å
34
SI InP Substrate
36
40
42
44
46
48

FIG. 1

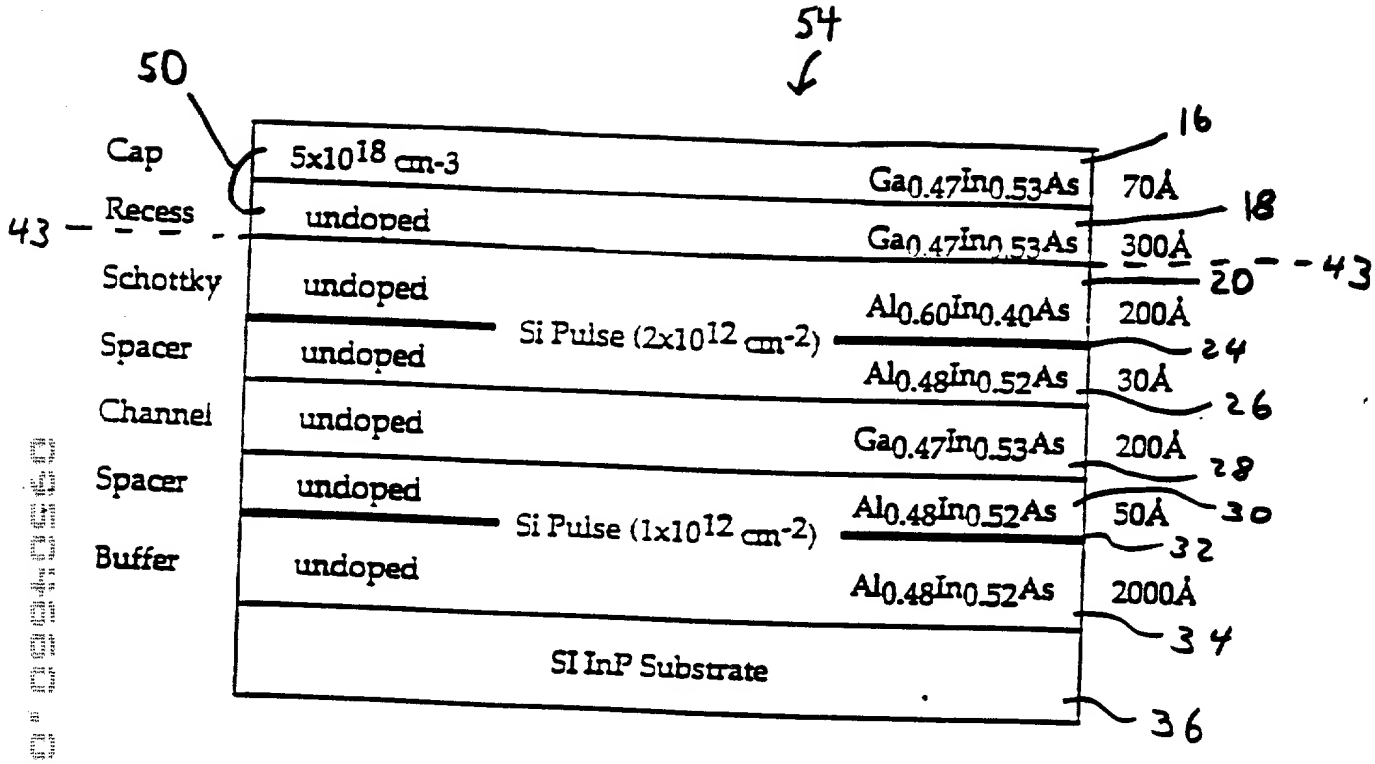
54
50
Cap
Recess
Schottky
Spacer
Channel
Spacer
Buffer
43
5x10^18 cm-3
undoped
undoped
undoped
undoped
undoped
undoped
Si Pulse (2x10^12 cm-2)
Si Pulse (1x10^12 cm-2)
Ga0.47In0.53As 70Å
Ga0.47In0.53As 300Å
Al0.60In0.40As 200Å
Al0.48In0.52As 30Å
Ga0.47In0.53As 200Å
Al0.48In0.52As 50Å
Al0.48In0.52As 2000Å
SI InP Substrate
16
18
20
43
24
26
28
30
32
34
36

FIG. 2

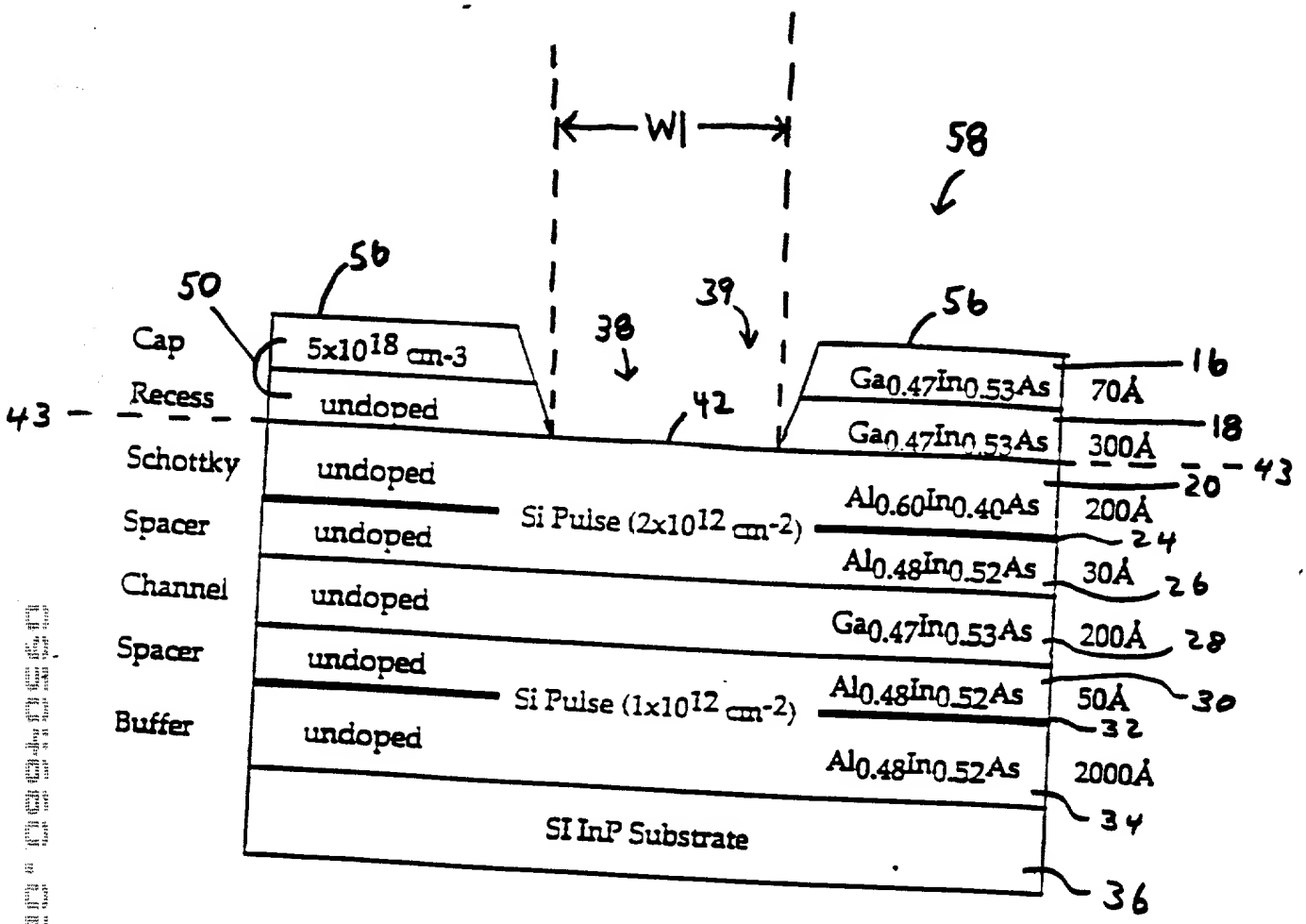
W
58
56
50
39
38
56
Cap
5x10^18 cm-3
Ga0.47In0.53As
70Å
16
43
Recess
undoped
42
Ga0.47In0.53As
300Å
18
Schottky
undoped
20
43
Al0.60In0.40As
200Å
Spacer
undoped
Si Pulse (2x10^12 cm-2)
24
Al0.48In0.52As
30Å
26
Channel
undoped
Ga0.47In0.53As
200Å
28
Spacer
undoped
Si Pulse (1x10^12 cm-2)
Al0.48In0.52As
50Å
30
32
Buffer
undoped
Al0.48In0.52As
2000Å
34
SI InP Substrate
36

FIG. 3

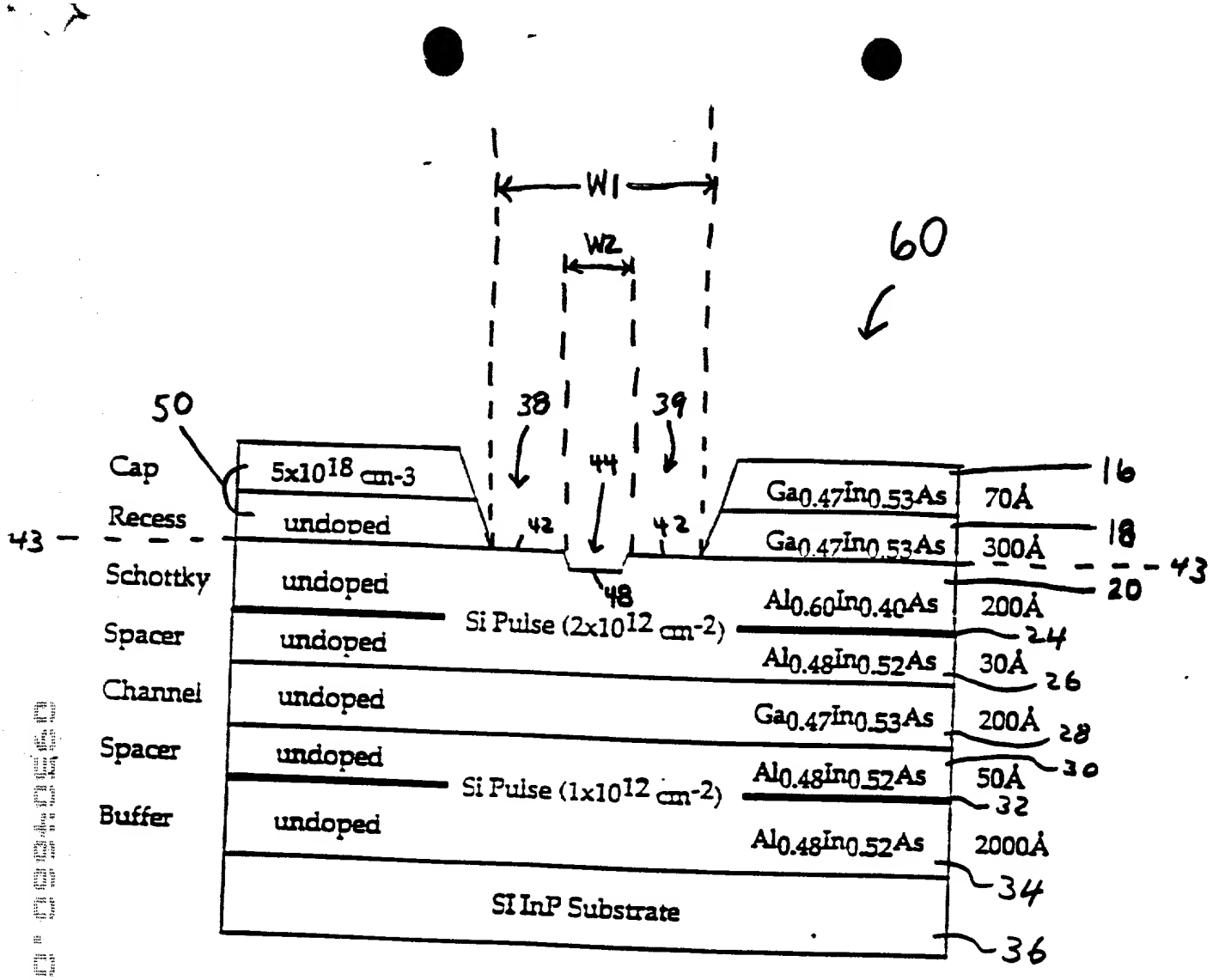
W1
W2
60
50
38
39
44
42
42
48
43
Cap
Recess
Schottky
Spacer
Channel
Spacer
Buffer
5x10^18 cm-3
undoped
undoped
undoped
undoped
undoped
undoped
Si Pulse (2x10^12 cm-2)
Si Pulse (1x10^12 cm-2)
SI InP Substrate
Ga0.47In0.53As 70Å 16
Ga0.47In0.53As 300Å 18
Al0.60In0.40As 200Å 20
Al0.48In0.52As 30Å 24
Ga0.47In0.53As 200Å 26
Al0.48In0.52As 50Å 28
Al0.48In0.52As 2000Å 30
32
34
36

FIG. 4

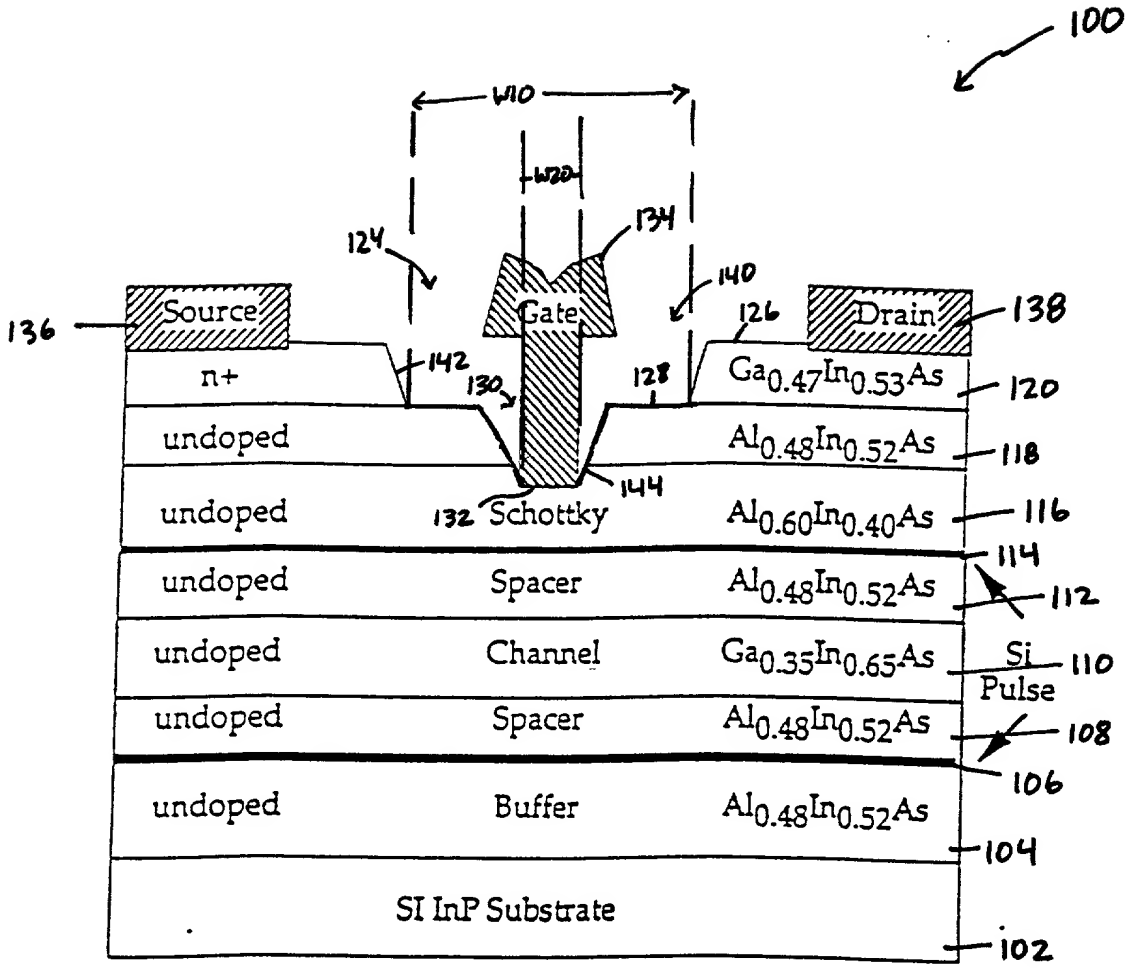
100
W10
W20
124
134
140
136
Source
Gate
Drain
138
126
142
130
128
n+
$Ga_{0.47}In_{0.53}As$
120
undoped
$Al_{0.48}In_{0.52}As$
118
undoped
132 Schottky
144
$Al_{0.60}In_{0.40}As$
116
114
undoped
Spacer
$Al_{0.48}In_{0.52}As$
112
undoped
Channel
$Ga_{0.35}In_{0.65}As$
Si
Pulse
110
undoped
Spacer
$Al_{0.48}In_{0.52}As$
108
106
undoped
Buffer
$Al_{0.48}In_{0.52}As$
104
SI InP Substrate
102

FIG. 5

Attorney's Docket No.: 07206-047001
Client's Ref. No.: 36827

COMBINED DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled DOUBLE RECESSED TRANSISTOR, the specification of which:

[X] is attached hereto.
[ ] was filed on _ as Application Serial No. _ and was amended on _____.
[ ] was described and claimed in PCT International Application No. _____ filed on _____ and as amended under PCT Article 19 on _____.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose all information I know to be material to patentability in accordance with Title 37, Code of Federal Regulations, §1.56.

I hereby appoint the following attorneys and/or agents to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith: Richard M. Sharkansky, Reg. No. 25,800; Tu N. Nguyen, Reg. No. 42,934; Eric L. Prahl, Reg. No. 32,590; Gary A. Walpert, Reg. No. 26,098; Andrew J. Rudd, Reg. No. 36,661; Glenn Lenzen, Reg. No. 29,320; Robin R. Longo, Reg. No. 40,071; and Deborah U. Verga, Reg. No. 38,351.

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patents issued thereon.

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